A 12-to-16-bit Column-Parallel CMS-based ADC for High Monotonically Linear Dynamic Range

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***Abstract*—This paper presents a 12-to16-bit column-parallel correlated multiple sampling (CMS)-based analog-to-digital converter (ADC), implemented in a 0.11 μm CMOS image sensor technology. The implemented image sensor has a resolution of 1080(H) x 1080(V) with a pixel pitch of 4.5 μm, and a die size of 9mm(H) x 10.44mm(V). The ADC features multiple per-cycle gains and 1.5b DAC per cycle. The measured peak temporal noise was reduced from 10.41 e-rms to 2.33 e-rms when varying the number of CMS from 4 to 64. By setting the analog gain to 4, the temporal noise was further reduced to 1.21 e-rms, at a conversion gain of 22.87 μV/e-. Additionally, the measured dark current distribution is 6.2 e-/s.**

Keywords—CMOS image sensor, column-parallel ADC, cumulative multiple sampling, high dynamic range, folding integration/cyclic ADC

I. Introduction

A column-parallel ADC with high gray-scale resolution and a highly monotonic-linear dynamic range is essential for CMOS imagers used in high-end digital still cameras (DSCs) and scientific applications. The ADC should effectively reduce noise from analog readout circuits, including source followers, by employing high-gain amplification. At the same time, it must preserve the intra-scene dynamic range, which is defined by the ratio between the noise level and the pixel's full-well capacity. Column-parallel ADC architectures using correlated multiple sampling (CMS) are one of the best ways to realize these requirements[1], [2], [3], [4], [5], [6].

In the CMS-based ADC using the cascaded operation of folding-integration and cyclic ADCs [4], the per-cycle gain of 0.5 and effective 1b digital-to-analog converter (DAC) per cycle in integration are used. This paper presents a CMS-based ADC featuring multiple per-cycle gains and 1.5b DAC per cycle.

II. Operation Principles

Figure 1a illustrates the phase diagram of the FI ADC, which operates at three different FI gain cycles. Initially, the input signal is connected to both capacitors C_1 and C_2 to achieve the gain setting of G=2 in the first cycle. The input is then connected to only C_1 to achieve the gain setting of G=1 in the subsequent cycles. In the final cycle, both C_{1a} and C_{1b} are connected to the low reference voltage, $V_{RL,}$ and the gain setting becomes G=0. Figure 1b summarizes the phases of the folding integration operation of the proposed ADC, where M denotes the number of cycles in the folding integration stage. The summation of the number of cycles multiplied by the respective gains corresponds to the total CMS gain.

Figure 2 shows the phase diagram of the cyclic ADC. In the first cycle, the analog input signal is sampled, as shown in Figure 2a. The integrator output is sampled and fed back to the input during the following cycles, as shown in Figure 2b. A 1.5b DAC per cycle is used to mitigate the effect of comparator nonlinearity error, denoted by D=0,1,2 in Figure 2b. Figure 3 shows the capability of the proposed ADC to have different modes by modifying the number of multiple samplings and cyclic ADC cycles. The flexibility allows the proposed ADC to realize two different modes, i.e. the low noise and the high-speed ADC modes, where the low noise mode (LN) has an extra bit in the FIADC, while the high-speed mode (HS) has an extra bit in cyclic operation. Each mode ranges from 12b to 16b resolution.

III. Measurement Results

The prototype chip was fabricated using 0.11 μm 1P4M CIS technology, featuring a pixel array of 1080(H) x 1080(V) with a pixel pitch of 4.5 μm, and a die size of 9mm(H) x 10.44mm(V). Figure 4a depicts the variation in temporal noise distribution with varying numbers of CMS from 4, 8, 16, 32, and 64, and an analog gain of 0.8. The peak temporal noise was reduced from 10.41 e-rms to 2.33 e-rms, verifying the effect of the CMS operation. Figure 4b compares the results for different variations of CMS and analog gain settings (Gain=0.8, 2, 4). By setting the CMS gain to 64 and analog gain to 4, the temporal noise was reduced to 1.21 e-rms, achieving 8.57 times noise reduction. Dark current distribution is shown in Figure 5, with the peak at 6.2 e-/s. The conversion gain obtained from the photon transfer curve is 22.87 μV/e-. Figure 7 shows the image taken using the proposed ADC using the low noise LN12b mode. Table 1 compares this work with the prior work of FI/C ADC. Compared to the conventional FI/C ADC, this ADC achieved a higher ADC dynamic range and very low input-referred voltage domain noise, which is essential for high-end cameras.

Acknowledgment

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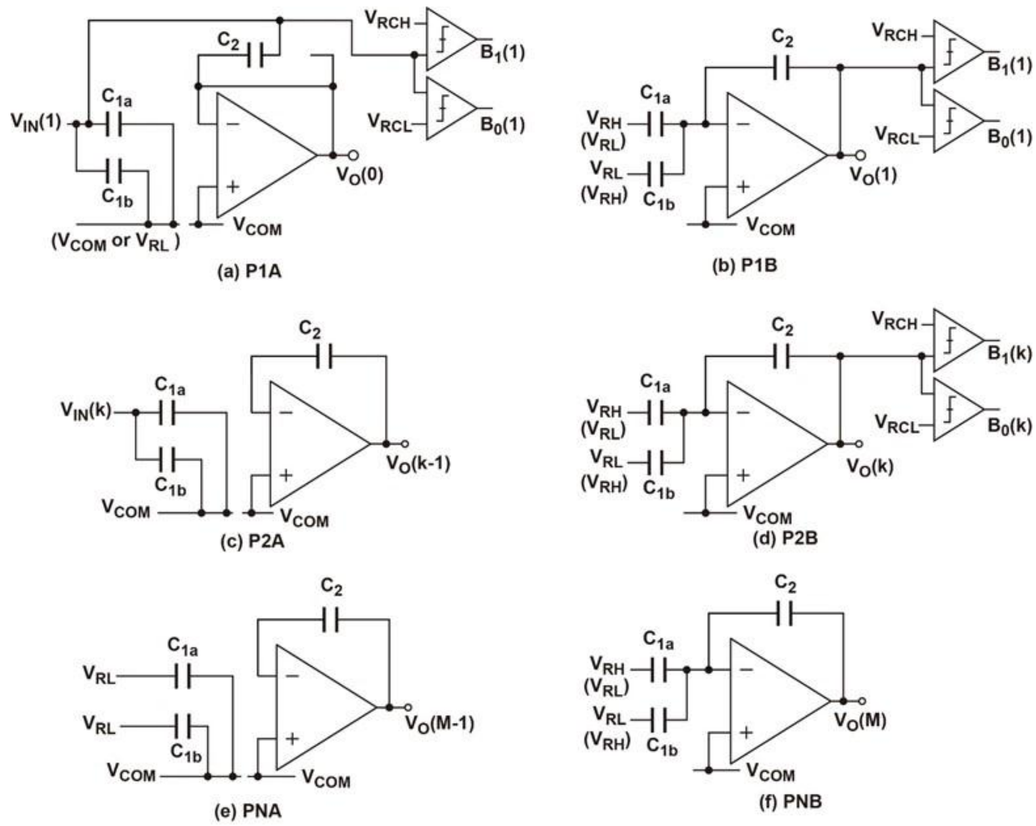
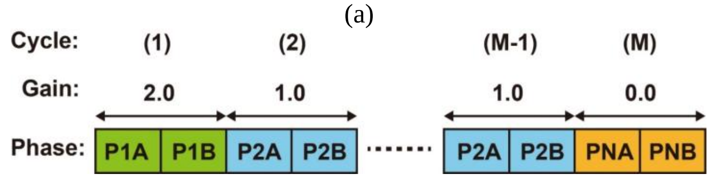


(a)



(b)

Figure 1: Phase diagram of the folding Integration operation.

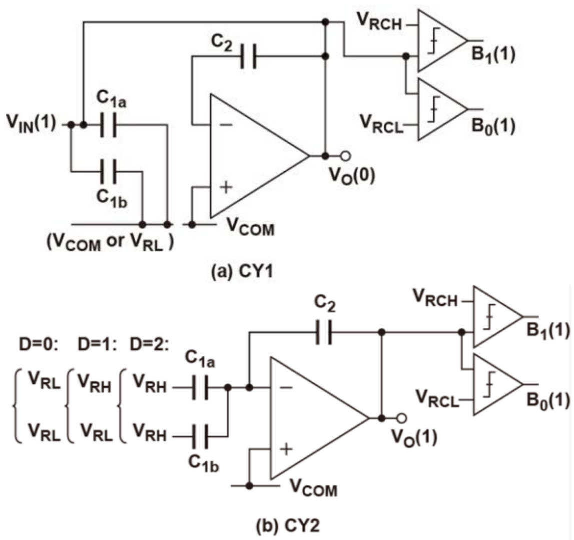
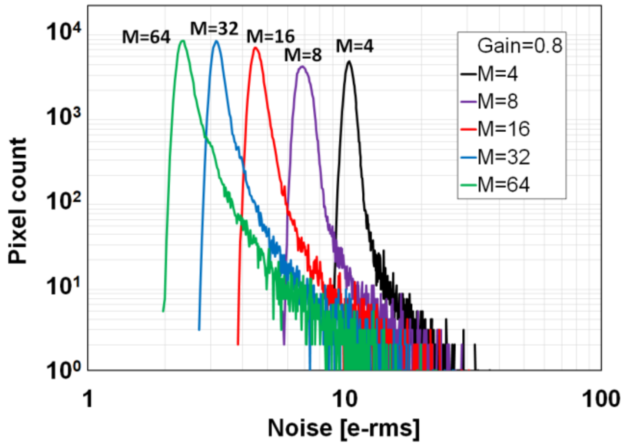


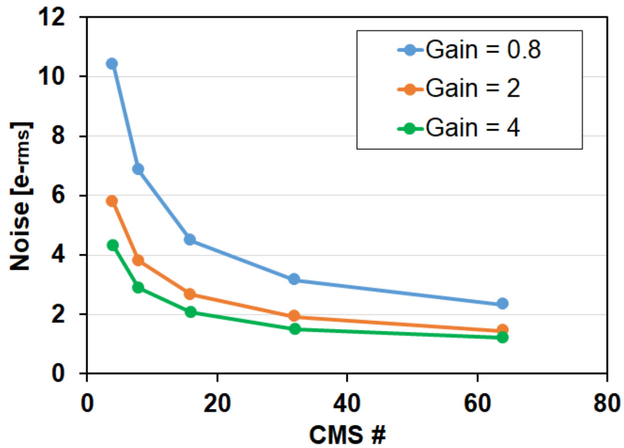
Figure 2: Phase diagram of the cyclic operation.

Mode	Mode Name	FIADC [bit]	Cyclic [bit]	Total [bit]	# of Cycles in FIADC			CMS Gain
					G=2	G=1	G=0	
Low Noise	LN12b	3	10	12	1	2	1	4
	LN13b	4	10	13	1	6	1	8
	LN14b	5	10	14	1	14	1	16
	LN15b	6	10	15	1	30	1	32
	LN16b	7	10	16	1	62	1	64
High Speed	HS12b	2	11	12	1	0	0	2
	HS13b	3	11	13	1	2	1	4
	HS14b	4	11	14	1	6	1	8
	HS15b	5	11	15	1	14	1	16
	HS16b	6	11	16	1	30	1	32

Figure 3: High speed and low noise ADC modes ranging from 12b to 16b resolution.



(a)



(b)

Figure 4: (a) The temporal noise distribution for CMS from 4 to 64 times. PGA gain is set to 0.8. (b) Comparison of variation of CMS and three settings of PGA gain showing the effectiveness of gain reduction with higher ADC resolution.

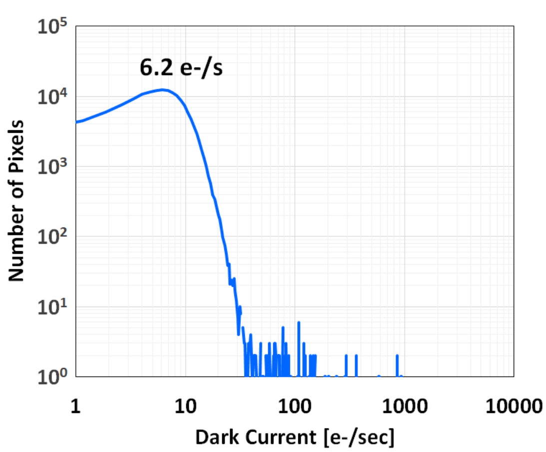


Figure 5: Dark current distribution showing the peak at 6.2 e-/s

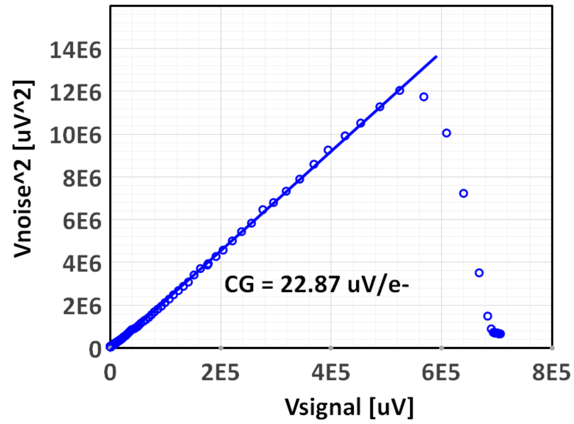


Figure 6: The photon transfer curve to obtain the conversion gain.

Figure 7: Image taken using the proposed ADC with LN12b mode.

		[4]	This work		
Process		110nm CIS	110nm CIS		
Pixel Size [μm]		7.5	4.5		
CG [μV/e-]		67	22.87		
Analog Gain		1	0.8	2	4
Temporal noise	[e_{rms}]	1.2	2.33	1.45	1.21
	[μV_{rms}]	80.4	53.2	33.2	27.7
Dynamic Range [dB]		82	87	84	79
CMS #		64	64		
ADC Resolution		18b	16b		

Table 1: Comparison table